

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		10001478
	Filing Date		2001-11-01
	First Named Inventor	Craig Nemecek	
	Art Unit	2123	
	Examiner Name	Jason Scott Pector /Dwin Craig/	
	Attorney Docket Number	CD01213M	

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
/D.C./	1	6910126	B1	2005-06-21	Mar et al.	Entire Document
/D.C./	2	6825689	B1	2004-11-30	Snyder	Entire Document
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/D.C./	5	6967511	B1	2005-11-22	Sullam	Entire Document
/D.C./	6	6892322	B1	2005-05-10	Snyder	Entire Document
/D.C./	7	6823282	B1	2004-11-23	Snyder	Entire Document
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Examiner Name	Jason Scott Proctor	/Dwin Craig/
Attorney Docket Number	CD01213M	

/D.C./	9	6611220	B1	2003-08-26	Snyder	Entire Document
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/D.C./	32	6608472	B1	2003-08-19	Kutz et al.	Entire Document
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/D.C./	1	USPTO Notice of Allowance for 10/238,966 (CD01250) dated 01/27/09; 4 pages	<input type="checkbox"/>

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/D.C./	2	USPTO Non-Final Rejection for 10/238,966 (CD01250) dated 06/30/08; 12 pages	<input type="checkbox"/>
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/D.C./	9	USPTO Non-Final Rejection for 10/033,027 (CD00232) dated 12/18/08; 5 pages	<input type="checkbox"/>
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/D.C./	13	USPTO Non-Final Rejection for 10/033,027 (CD00232) dated 04/26/06; 26 pages	<input type="checkbox"/>
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/D.C./	35	USPTO Non-Final Rejection for 10/002,217 (CD01207) dated 05/19/05; 15 pages	<input type="checkbox"/>
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/D.C./	37	USPTO Advisory Action for 10/001,477 (CD01203) dated 10/10/08; 3 pages	<input type="checkbox"/>
/D.C./	38	USPTO Final Rejection for 10/001,477 (CD01203) dated 06/30/08; 15 pages	<input type="checkbox"/>
/D.C./	39	USPTO Non-Final Rejection for 10/001,477 (CD01203) dated 12/06/07; 13 pages	<input type="checkbox"/>
/D.C./	40	USPTO Final Rejection for 10/001,477 (CD01203) dated 07/23/07; 16 pages	<input type="checkbox"/>
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EXAMINER SIGNATURE

Examiner Signature	/Dwin Craig/	Date Considered	10/13/2011
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Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

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/D.C./	9	6249167	B1	2001-06-19	Oguchi et al.	Entire Document
/D.C./	10	4134073	B1	1979-01-01	MacGregor	Entire Document
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/D.C./	20	5331571	B1	1994-07-19	Aronoff et al.	Entire Document
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Examiner Name	Jason Scott Proctor /Dwin Craig/	
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	33	Application Number 09/943,062 (CD00228): "Apparatus and Method for Programmable Power Management in a Programmable Analog Circuit Block;" Mar; 46 pages	<input type="checkbox"/>
	34	Application Number 10/238,966 (CD01250M); "Method for Parameterizing a User Module;" Penn; 41 pages	<input type="checkbox"/>
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	48	Application Number 09/207,912 (CD98086): "Circuit(s), Architecture and Method(s) for Operating and/or Tuning a Ring Oscillator," Mar; 23 pages	<input type="checkbox"/>
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/D.C./	1	6681280	B1	2004-01-20	Miyake, et al.	Entire Document
/D.C./	2	5399922	B1	1995-03-21	Kiani et al.	Entire Document
/D.C./	3	5680070	B1	1997-10-21	Anderson et al.	Entire Document
/D.C./	4	6314530	B1	2001-11-06	Mann	Entire Document
/D.C./	5	5438672	B1	1995-08-01	Dey	Entire Document
/D.C./	6	6166367	B1	2000-12-26	Cho	Entire Document
/D.C./	7	5600262	B1	1997-02-04	Kolze	Entire Document
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/D.C./	9	5258760	B1	1993-11-02	Moody et al.	Entire Document
/D.C./	10	5563526	B1	1996-10-08	Hastings et al.	Entire Document
/D.C./	11	6225866	B1	2001-05-01	Kubota et al.	Entire Document
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/D.C./	15	5828693	B1	1998-10-27	Mays et al.	Entire Document
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/D.C./	23	5050168	B1	1991-09-17	Paterson	Entire Document
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/D.C./	2	0450863A2	EP	A1	1991-10-09	Austin	Entire Document	<input type="checkbox"/>
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/D.C./	13	06021732	JP	A1	1994-01-28	Kadowaki, Tadao	Entire Document	<input type="checkbox"/>

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/D.C./	1	From Application Number 10/033,027 (CD00232): Goodenough, F. "Analog Counterparts of FPGAS Ease System Design" Electronic Design, Penton Publishing, Cleveland, OH, US vol. 42, no. 21, 10/14/94; 10 pages	<input type="checkbox"/>
/D.C./	2	From Application Number 10/033,027 (CD00232): Harbaum, T. et al. "Design of a Flexible Coprocessor Unit" Proceedings of the Euromicro Conference, XX XX, Sept. 1999; 10 pages	<input type="checkbox"/>
/D.C./	3	From Application Number 10/033,027; CD00169: "Programmable Microcontroller (PSoC) Architecture (Mixed Analog/Digital)"; 08/07/01; 09/924,734 Snyder et al.; 28 pages	<input type="checkbox"/>
/D.C./	4	From Application Number 10/033,027; CD00170: "Digital Configurable Macro Architecture"; 07/18/01; 09/909,045; Snyder; 37 pages	<input type="checkbox"/>

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/D.C./	5	From Application Number 10/033,027: CD00172; "Configuring Digital Functions in a Digital Configurable Macro Architecture"; 07/18/01; 09/909,109; Snyder; 38 pages	<input type="checkbox"/>
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/D.C./	8	From Application Number 10/033,027: CD00175; "Method for Synchronizing and Resetting Clock Signals Supplied to Multiple Programmable Analog Blocks (As Amended)"; 10/01/01; 09/969,311; Sullam; 57 pages	<input type="checkbox"/>
/D.C./	9	From Application Number 10/033,027: CD00180; "Method and Apparatus for Programming a Flash Memory"; 06/05/01; 09/875,599; Snyder; 23 pages	<input type="checkbox"/>
/D.C./	10	From Application Number 10/033,027: CD00182; "In-System Chip Emulator Architecture"; 10/10/01; 09/975,115; Snyder et al.; 38 pages	<input type="checkbox"/>
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/D.C./	12	From Application Number 10/033,027: CD00199; "Multiple Use of Microcontroller Pad"; 06/26/01; 09/893,050; Kutz et al.; 21 pages	<input type="checkbox"/>
/D.C./	13	From Application Number 10/033,027: CD00226; "Programming Architecture for a Programmable Analog System"; 08/14/01; 09/929,891; Mar et al.; 82 pages	<input type="checkbox"/>
/D.C./	14	From Application Number 10/033,027 (CD00227): "Architecture for Synchronizing and Resetting Clock Signals Supplied to Multiple Analog Programmable Analog Blocks"; 10/01/01; 09/969,313; Sullam; 50 pages	<input type="checkbox"/>
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/D.C./	20	GANAPATHY, GOPI, AND NARAYAN, RAM, AND JORDEN, GLEN, AND FERNANDEZ, DENZIL, AND WANG, MING, AND NISHIMURA, JIM; "Hardware Emulation for Functional Verification of K5", June 1996, 33rd Design Automation Conference Proceedings, 3-7 June 1996; 4 pages	<input type="checkbox"/>
	21	The Provisional Application 60/243,708 (CD00167D); "Advanced Programmable Microcontroller Device"; 277 pages	<input type="checkbox"/>
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	24	Application Number 09/057,084 (CD00204); "A Crystal-Less Oscillator with Trimmable Analog Current Control for Increased Stability;" Mar; 28 pages	<input type="checkbox"/>
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27	Application Number 09/972,003 (CD00176): "Test Architecture for Microcontroller Providing for a Serial Communication Interface;" Snyder; 32 pages	<input type="checkbox"/>
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38	Application Number 10/004,039 (CD01222M): "In-Circuit Emulator with Gatekeeper for Watchdog Timer;" Nemecek; 46 pages	<input type="checkbox"/>
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40	Application Number 10/001,568 (CD01214M): "Combined In-Circuit Emulator and Programmer;" Nemecek; 47 pages	<input type="checkbox"/>
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49	Application Number 09/935,454 (CD00194); "Method and Apparatus for Local and Global Power Management in a Programmable Analog Circuit;" Mar; 51 pages	<input type="checkbox"/>
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/D.C./	4	Nam et al.; "Fast Development of Source-Level Debugging System Using Hardware Emulation"; IEEE 2000; 4 pages	<input type="checkbox"/>
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↑	14	Sedory; "A Guide to Debug"; 2004; retrieved on May 20, 2005; 7 pages	<input type="checkbox"/>
↑	15	"Microsoft Files Summary Judgement Motions"; February 1999; Microsoft PressPass; retrieved on May 20, 2005 from http://www.microsoft.com/presspass/press/1999/feb99/Feb99/Calderapr.asp ; 3 pages	<input type="checkbox"/>
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↑	17	Stallman et al.; "Debugging with the GNU Source-Level Debugger"; January 1994; retrieved on May 2, 2005 from http://www.cs.utah.edu ; 4 pages	<input type="checkbox"/>
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↑	19	Stan Augarten; "The Chip Collection - Introduction - Smithsonian Institute"; "State of the Art"; "The First 256-Bit Static RAM"; retrieved on November 14, 2005 from http://smithsonianchips.si.edu/augarten/p24.htm ; 2 pages	<input type="checkbox"/>
↑	20	"POD - Piece of Data, Plain Old Documentation, Plain Old Dos..."; retrieved on November 14, 2005 from http://www.auditmypc.com/acronym/POD.asp ; 2 pages	<input type="checkbox"/>
↑	21	USPTO Non-Final Rejection for 09/989,767 (CD01178M) dated 10/06/04; 15 pages	<input type="checkbox"/>
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Application Number		10001478
Filing Date		2001-11-01
First Named Inventor	Craig Nemecek	
Art Unit	2123	
Examiner Name	Jason Scott Proctor /Dwin Craig/	
Attorney Docket Number	CD01213M	

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	4	7376904	B1	2008-05-20	Cifra et al.	Entire Document
	5	7024654	B1	2006-04-04	Bersch et al.	Entire Document
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/D.C./	2	"pod-defintion by dict.die.net"; retrieved on November 14, 2005 from http://dict.die.net/pod ; 2 pages	<input type="checkbox"/>
	3	"In-Circuit Emulators - descriptions of the major ICEs around"; retrieved on November 14, 2005 from http://www.algonet.se/~staffann/developer/emulator.htm ; 6 pages	<input type="checkbox"/>
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Attorney Docket Number	CD01213M

/D.C./	5	USPTO Non-Final Rejection for 09/989,767 (CD01178M) dated 07/24/08; 21 pages	<input type="checkbox"/>
/D.C./	6	Anonymous; "Using Debug"; 1999; Prentice-Hall Publishing; 20 pages	<input type="checkbox"/>
/D.C./	7	Harrison et al.; "Xilinx FPGA Design in a Group Environment Using VHDS and Synthesis Tools"; Colloquium on Digital System Design Using Synthesis Techniques; February 15, 1996; 4 pages	<input type="checkbox"/>
/D.C./	8	Microsoft Press Computer User's Dictionary; 1998; 3 pages	<input type="checkbox"/>
/D.C./	9	Sreeram Duvvuru and Siamak Arya, "Evaluation of a Branch Target Address Cache," 1995; IEEE; 8 pages	<input type="checkbox"/>
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/D.C./	11	USPTO Non-Final Rejection for 09/989,767 (CD01178M) dated 07/17/06; 12 pages	<input type="checkbox"/>
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
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Application Number	10001478
Filing Date	2001-11-01
First Named Inventor	Craig Nemecek
Art Unit	2123
Examiner Name	Jason Scott Proctor /Dwin Craig/
Attorney Docket Number	CD01213M

/D.C./	1	USPTO Notice of Allowance for 09/992,076 (CD01210M) dated 11/13/2008; 15 pages	<input type="checkbox"/>
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First Named Inventor	Craig Nemecek
Art Unit	2123
Examiner Name	Jason Scott Proctor /Dwin Craig/
Attorney Docket Number	CD01213M

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/D.C./	16	USPTO Non-Final Rejection for Application Number 09/969,311 (CD00175) dated 09/21/2004; 4 pages	<input type="checkbox"/>

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Application Number	10001478
Filing Date	2001-11-01
First Named Inventor	Craig Nemecek
Art Unit	2123
Examiner Name	Jason Scott Proctor /Dwin Craig/
Attorney Docket Number	CD01213M

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/D.C./	1	6934674	B1	2005-08-23	Douezzy et al.	Entire Document
/D.C./	2	6051772	B1	2000-04-18	Cameron et al.	Entire Document
/D.C./	3	6016554	B1	2000-01-18	Skrovan et al.	Entire Document
/D.C./	4	6704889	B1	2004-03-09	Veenstra et al.	Entire Document
/D.C./	5	5978937	B1	1999-11-02	Miyamori et al.	Entire Document
/D.C./	6	5317202	B1	1994-05-31	Waizman	Entire Document
/D.C./	7	6121805	B1	2000-09-19	Thamsirianunt et al.	Entire Document
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/D.C./	9	6396302	B1	2002-05-28	New et al.	Entire Document
/D.C./	10	6204687	B1	2001-03-20	Schultz et al.	Entire Document
/D.C./	11	5996032	B1	1999-11-30	Baker	Entire Document
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/D.C./	14	5949632	B1	1999-09-07	Barreras Sr. et al.	Entire Document
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/D.C./	21	6166960	B1	2000-12-26	Marneweck et al.	Entire Document
/D.C./	22	5982105	B1	1999-11-09	Masters	Entire Document
/D.C./	23	4740966	B1	1988-04-26	Goad	Entire Document
/D.C./	24	6643151	B1	2003-11-04	Nebrigic et al.	Entire Document
/D.C./	25	6003133	B1	1999-12-14	Moughanni et al.	Entire Document
/D.C./	26	6339815	B1	2002-01-15	Feng et al.	Entire Document
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/D.C./	28	5737760	B1	1998-04-07	Grimmer et al.	Entire Document
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/D.C./	31	6839774	B1	2005-01-04	Ahn et al.	Entire Document
/D.C./	32	6754765	B1	2004-06-22	Chang et al.	Entire Document
/D.C./	33	5630057	B1	1997-05-13	Hait	Entire Document
/D.C./	34	6324628	B1	2001-11-27	Chan	Entire Document
/D.C./	35	6236593	B1	2001-05-22	Hong et al.	Entire Document
/D.C./	36	6219729	B1	2001-04-17	Keats et al.	Entire Document
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/D.C./	38	5378935	B1	1995-01-03	Korhonen et al.	Entire Document
/D.C./	39	5572719	B1	1996-11-05	Biesterfeldt	Entire Document
/D.C./	40	5579353	B1	1996-11-26	Parmenter et al.	Entire Document
/D.C./	41	5696952	B1	1997-12-09	Pontarelli	Entire Document

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/D.C./	42	5774704	B1	1998-06-30	Williams	Entire Document
/D.C./	43	5986479	B1	1999-11-16	Mohan, Jitendra	Entire Document
/D.C./	44	6603348	B1	2003-08-05	Preuss et al.	Entire Document

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/D.C./	2	20020059543	A1	2002-05-16	Cheng et al.	Entire Document
/D.C./	3	20010010083	A1	2001-07-26	Satoh	Entire Document
/D.C./	4	20020133794	A1	2002-09-19	Kanapathippillai et al.	Entire Document
/D.C./	5	20020065646	A1	2002-05-30	Waldie et al.	Entire Document
/D.C./	6	20020133771	A1	2002-09-19	Barnett	Entire Document

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Examiner Name	Jason Scott Proctor /Dwin Craig/
Attorney Docket Number	CD01213M

/D.C./	6	USPTO Non-Final Rejection for Application Number 11/644,100 (CD05204) dated 04/14/2008; 10 pages	<input type="checkbox"/>
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	13	Application Number 11/644,100 (CD05204): "Differential to single ended signal converter circuit and method," Sun, 33 pages	<input type="checkbox"/>
	14	Application Number 11/415,588 (CD05028): "Voltage Controlled Oscillator Delay Cell and Method," Sivadasan, 24 pages	<input type="checkbox"/>
	15	Application Number 12/218,404 (CD05028C1): "Voltage Controlled Oscillator Delay Cell and Method," Sivadasan, 23 pages	<input type="checkbox"/>
/D.C./	16	USPTO Notice of Allowance for Application Number 11/132,894 (CD04064) dated 04/26/2007; 4 pages	<input type="checkbox"/>

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/D.C./	17	USPTO Non-Final Rejection for Application Number 11/132,894 (CD04064) dated 12/19/2006; 12 pages	<input type="checkbox"/>
	18	Application Number 11/132,894 (CD04064): "Open Loop Bandwidth Test Architecture and Method for Phase Locked Loop (PLL)," Stiff, 38 pages	<input type="checkbox"/>
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	25	Application Number 11/322,044 (CD05198): "Self charge pump PLL architecture," Stiff, 10 pages	<input type="checkbox"/>
/D.C./	26	USPTO Notice of Allowance for Application Number 10/305,589 (CD02181) dated 02/04/2005; 5 pages	<input type="checkbox"/>
/D.C./	27	USPTO Final Rejection for Application Number 10/305,589 (CD02181) dated 10/21/2004; 7 pages	<input type="checkbox"/>

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	29	Application Number 10/305,589 (CD02181): "Current Controlled Delay Circuit," Stiff, 10 pages	<input type="checkbox"/>
	30	Application Number 00/940,464 (CD04035): "Reduced State Phase Error CMOS PLL Charge Pump," Stiff, 30 pages	<input type="checkbox"/>
/D.C./	31	Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996; 10 pages	<input type="checkbox"/>
/D.C./	32	Larsson, "A 2-1600-MHz CMOS Clock Recovery PLL with Low-V _{dd} Capability," IEEE Journal of Solid-State Circuits, Vol. 34, No. 12, December 1999; 10 pages	<input type="checkbox"/>
/D.C./	33	USPTO Notice of Allowance for Application Number 10/327,217 (CD02174) dated 08/12/2004; 6 pages	<input type="checkbox"/>
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	36	Application Number 10/327,217 (CD02174): "Single Ended Clock Signal Generator Having a Differential Output," Richmond et al., 27 pages	<input type="checkbox"/>
/D.C./	37	USPTO Notice of Allowance for Application Number 10/871,582 (CD03036) dated 03/30/2006; 6 pages	<input type="checkbox"/>
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/D.C./	3	6680632	B1	2004-01-20	Meyers et al.	Entire Document
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	14	6949984	B1	2005-09-27	Siniscalchi	Entire Document
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	24	6670852	B1	2003-12-30	Hauck	Entire Document
	25	6625765	B1	2003-09-23	Krishnan	Entire Document
	26	6433645	B1	2002-08-13	Mann et al.	Entire Document
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/D.C./	45	7015735	B1	2006-03-21	Kimura et al.	Entire Document
/D.C./	46	6600351	B1	2003-07-29	Bisanti et al.	Entire Document
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/D.C./	8	Durham et al., "Circuit Architectures for High Linearity Monolithic Continuous-Time Filtering," IEEE, 1992; 7 pages	<input type="checkbox"/>
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	10	Application Number 09/047,595 (CD97115): "Roving Range Control to Limit Receive PLL Frequency of Operation," Scott; 35 pages	<input type="checkbox"/>
	11	Application Number 09/216,460 (CD98099): "Circuit and Method for Controlling an Output of a Ring Oscillator," Abugharbieh et al.; 21 pages	<input type="checkbox"/>
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	14	Application Number 10/083,442 (CD01264): "Method/Architecture for a Low Gain PLL with Wide Frequency Range," Meyers et al.; 28 pages	<input type="checkbox"/>
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	16	Application Number 09/893,161 (CD00094): "Architecture of a PLL with Dynamic Frequency Control on a PLD," Moore; 32 pages	<input type="checkbox"/>
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	19	Application Number 08/747,262 (CD00005): "Linearized Digital Phase-Locked Loop," Williams et al., 9 pages	<input type="checkbox"/>
	20	Application Number 09/001,440 (CD01102): "Oscillator Tuning Method," Hauck, 28 pages	<input type="checkbox"/>
	21	Application Number 08/538,886 (CD00104): "Memory Based Phase Locked Loop," Krishnan, 27 pages	<input type="checkbox"/>
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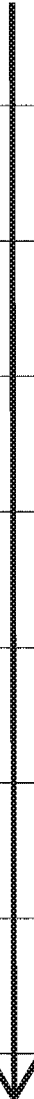

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Art Unit	2123
Examiner Name	Jason Scott Proctor /Dwin Craig/
Attorney Docket Number	CD01213M

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/D.C./	1	USPTO Advisory Action for Application Number 11/200,619 (CD04112) dated 05/11/2009; 3 pages	<input type="checkbox"/>
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/D.C./	6	USPTO Non-Final Rejection for Application Number 11/201,922 (CD04111) dated 10/21/2008; 12 pages	<input type="checkbox"/>
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/D.C./	10	USPTO Non-Final Rejection for Application Number 11/201,627 (CD04109) dated 12/12/2008; 17 pages	<input type="checkbox"/>
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/D.C./	12	USPTO Non-Final Rejection for Application Number 11/201,627 (CD04109) dated 11/16/2007; 16 pages	<input type="checkbox"/>
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	17	Application Number 09/989,808 (CD01169M): "Automatic generation of application program interfaces, source code, interrupts, and data sheets for microcontroller programming," Bartz et al.; 67 pages	<input type="checkbox"/>
/D.C./	18	USPTO Notice of Allowance for Application Number 10/109,979 (CD01211M) dated 03/14/2006; 6 pages	<input type="checkbox"/>
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/D.C./	28	USPTO Final Rejection for Application Number 09/989,761 (CD01179M) dated 08/26/2004; 7 pages	<input type="checkbox"/>
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/D.C./	39	PCT International Search Report of the International Searching Authority for PCT/US05/28793, filed 08/12/2005, mailed 11/19/2007; 5 pages	<input type="checkbox"/>
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/D.C./	9	6246410	B1	2001-06-12	Bergeron et al.	Entire Document
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(Not for submission under 37 CFR 1.99)

Application Number	10001478
Filing Date	2001-11-01
First Named Inventor	Craig Nemecek
Art Unit	2123
Examiner Name	Jason Scott Proctor /Dwin Craig/
Attorney Docket Number	CD01213M

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
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